

# FEATURING

## Improved Picture Quality Technologies Support High-Speed CMOS Sensors **Ultrahigh-Speed High Picture Quality CMOS Sensors Using Column-Parallel A/D Conversion**

- Ultrahigh-speed imaging using column-parallel A/D conversion
- High picture quality using a column-parallel digital CDS\*1 technique

\*1: CDS: Correlated double sampling

CMOS sensors are now widely used in cellular phones and other mobile devices, and as a result, sales of these devices have been increasing rapidly. Furthermore, demand for CMOS sensors has been increasing in fields that require high-speed imaging functions, such as digital single-lens reflex cameras.

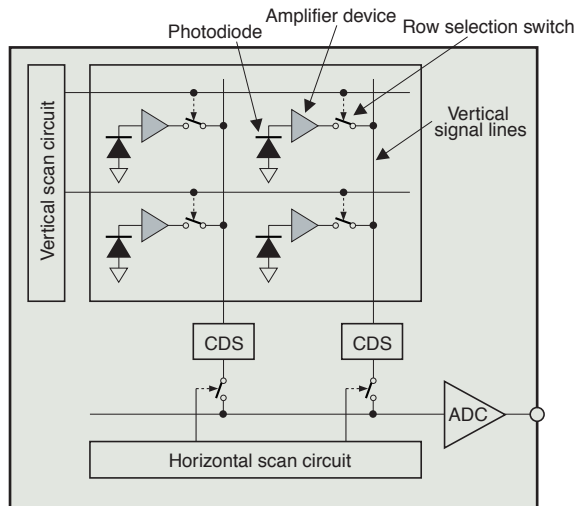
While CMOS sensor advantages over CCD include lower power consumption and higher speed, their main strength is in the possibilities for system integration, since analog and digital circuits can be integrated on the same chip. CMOS sensor can achieve high-speed characteristics that could not be achieved with CCD technology and can provide superb image quality that surpasses that of CCDs by taking advantage of these characteristics. Sony has now implemented a CMOS sensor that achieves both high-speed image readout and improved image quality by taking advantage of these CMOS sensor characteristics and integrating column-parallel A/D converters on the same chip. This CMOS sensor can read out 2.8M-pixel images at the speed of 180 frame/s.

Furthermore, this device achieves noise levels comparable to those of CCD image sensors at the same time as providing this high-speed readout.

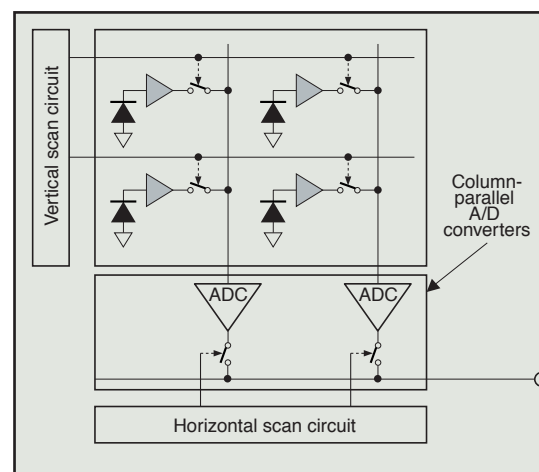
This article presents the high-speed imaging technology based on column-parallel A/D conversion and the noise reduction technology used in this device.

### The Column-Parallel A/D Conversion Technique

The possibility of system integration is a major feature of the CMOS sensor technology. It is possible to integrate both analog and digital circuits on the same chip as the pixel array used to capture images. Conventional CMOS sensors implemented noise cancellation using analog CDS circuits, and furthermore provided digital outputs by integrating A/D converters on the same chip. (See figure 1.) An amplifier device is embedded in each pixel in the CMOS sensor pixel circuit, and light is converted to an electrical signal by amplifying the signal



■ Figure 1 Conventional CMOS Sensor Circuit Structure



■ Figure 2 Column-Parallel A/D Converter CMOS Sensor Circuit Structure

charge generated by photodiode optoelectronic conversion. The pixel electrical signals selected by the vertical scan circuit are read out over the vertical signal lines. Since the signal is amplified at the pixel in the pixel structure that includes an amplifier, it is possible to design sensors in which the signal is relatively immune to the influence of noise on the signal path. On the other hand, since each pixel has its own amplifier, variations in device characteristics between pixels do occur. These variations are removed using a CDS circuit that samples both the reset state signal and the data signal and subtracts them. In the conventional circuit structure, the pixel signal from which the noise has been cancelled is temporarily stored in a memory capacitor. The analog signals stored in the CDS circuit are sequentially read out by the horizontal scan circuit and converted to digital signals by A/D converters integrated in the device. Until now, CMOS sensor functionality has been significantly improved by integrating the analog CDS circuits and the A/D convert-

ers on the same chip along with the CMOS sensor itself.

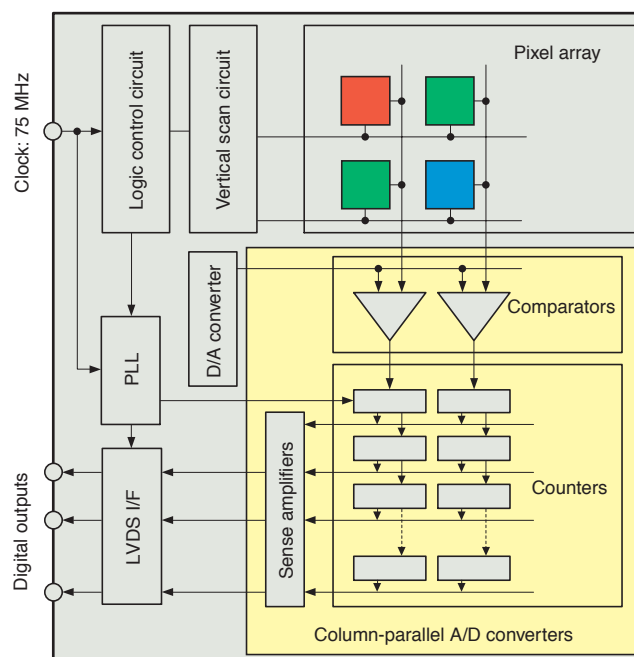
At the same time, however, the following problems occur in conventional CMOS sensors. Although the fixed pattern noise between pixels can be removed by the CDS circuits located at each column, a vertical form of fixed pattern noise occurs due to differences between the CDS circuits themselves.

Also a capacitor with a size larger than a certain value is required in the CDS circuit to record and hold the post-CDS signal, and this results in an increase in the area of this circuit. Furthermore, the recorded and stored analog signals are easily influenced by switching noise in the high-frequency band due to the horizontal transfer operations.

To resolve these problems, Sony adopted the column-parallel A/D conversion technique. (See figure 2.) Since each column has its own A/D converter in the column-parallel A/D conversion technique, the analog signals read out from the vertical signal lines can be A/D converted directly.

Since the analog signals are A/D converted directly without first recording and storing, the capacitors that take up chip area as circuit structural components are no longer required. Also, the analog CDS circuits used for noise cancellation are no longer required. The CDS operation previously performed with analog signal processing is now performed with digital processing. This technique makes it possible to perform high precision noise cancellation that is not dependent on variations in the CDS circuits.

Another advantage of the column-parallel A/D converter technique lies in its conversion speed. Since processing is performed in parallel for each column, the A/D conversion frequency is extremely low, and the high-frequency band noise components can be separated from the signal components. This means that even if the number of pixels or the frame rate are increased, high picture quality digital signals with extremely low noise can be acquired.

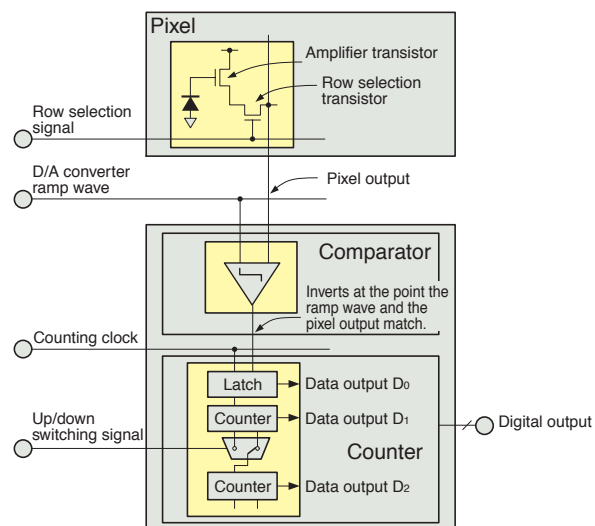


■ Figure 3 System Block Diagram

A column-parallel A/D converter CMOS sensor consists of the following six components.

1. Pixel array
2. Vertical scan circuit
3. Column-parallel A/D converter
4. D/A converter that generates a ramp wave
5. Logic control block
6. Digital output LVDS interface

Figure 3 shows the block diagram for the column-parallel A/D converter CMOS sensor. The CMOS sensor shown here operates from a single 75 MHz master clock. An internal PLL circuit generates a 300 MHz high-speed clock that is four times the frequency of the master clock to implement the high-speed operation of the column-parallel A/D converter, the slope generating D/A converter, and the LVDS interface.



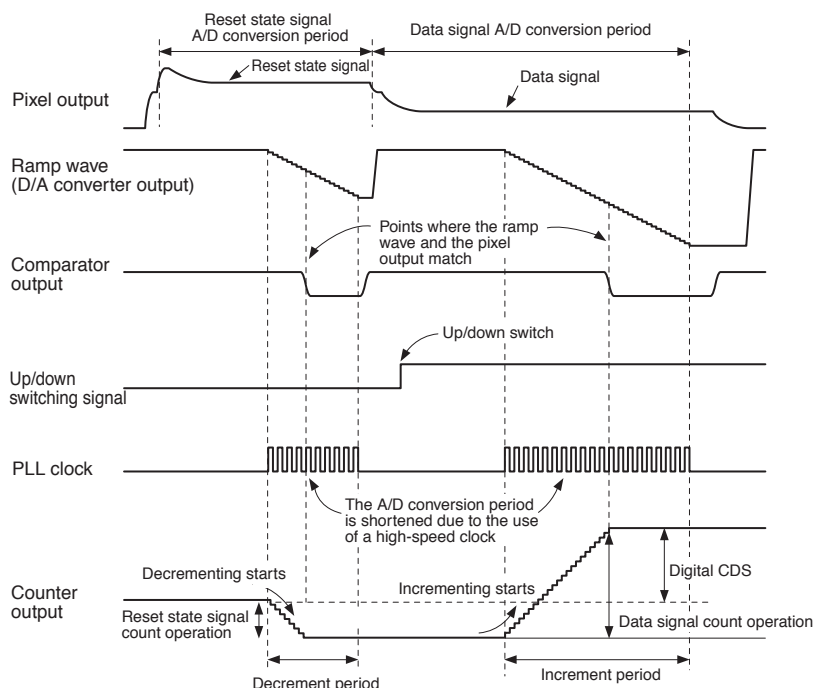
■ Figure 4 Column-Parallel A/D Conversion Technique

## Column-Parallel Digital CDS Technique

In the Sony-proposed column-parallel CDS technique, digital dual sampling (digital CDS) using the high-speed clock makes both high-speed readout and high picture quality possible. The column-parallel A/D converter consists of comparators and counters. (See figure 4.) The comparators in each column compare the ramp wave generated by the D/A converter with the pixel output. The counters in the columns are implemented as ripple counters and count the number of clocks until the comparator output changes. The subtraction of two digital signals can then be implemented by counting down during the reset state signal period and counting up during the data signal period. The digital CDS uses the high-speed 300 MHz clock and shortens the A/D conversion sampling period.

The column-parallel digital CDS technique operating sequence is as follows. (See figure 5.)

1. Pixels are reset and the pixel reset state signal is output to the vertical signal lines.
2. PLL clock cycles are counted until the ramp wave matches the pixel output and a reset state signal A/D conversion is performed. Here the ripple counter is set to decrement count operation by the up/down switching signal.
3. Data signals are output from the pixels. At this point, the ripple counter is set to increment count operation by the up/down switching signal.
4. An A/D conversion of the same type as that of step 2 is performed and as a result the counter output indicates a value that is the value of subtracting the reset state signal from the data signal (digital CDS). Signals read out from the pixels are processed in a column-parallel manner.



■ Figure 5 Column-Parallel A/D Converter Technique Timing Chart

- The digital CDS operation terminates and the digital data is transferred to the latch circuit that is present in each counter block. This allows the A/D conversion of the next row and the horizontal data transfers to be performed in a pipelined manner.

### Prototype Chip

Figure 6 shows a photograph of this prototype CMOS sensor chip. It supports an optical size with a diagonal of 8.7 mm (Type 1/1.8) and has a chip size of 7.0 (H) mm × 5.2 (V) mm. A 0.18 μm rule single polysilicon layer/three metal layer CMOS process is used.

Photograph 1 shows a sample image taken at 180 frame/s. The noise levels in this CMOS sensor that uses the column-parallel A/D conversion technique are almost the same at 180 frame/s and 45 frame/s.

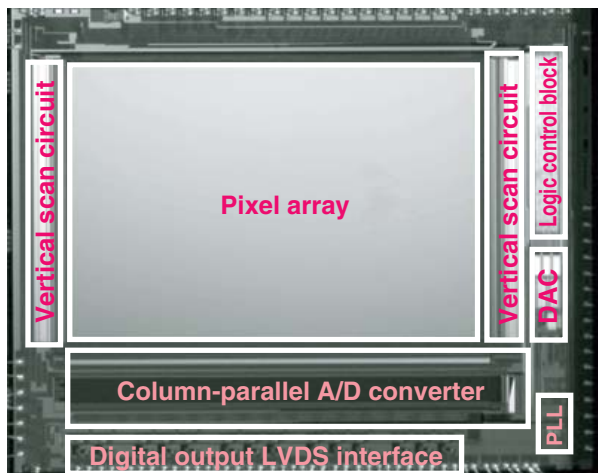
There is almost no recognizable image degradation when switching from 45 frame/s to 180 frame/s. Also, although the image distortion due to the focal plane shutter, which is a characteristic of CMOS sensors can be seen in the image taken at 45 frame/s, this distortion is almost invisible in the image taken at 180 frame/s. (See photograph 2.)

### Future Developments

The column-parallel A/D conversion technique introduced in this article achieves radical improvements in the speed and picture quality of CMOS sensors. Sony is now developing CMOS sensors that adopt this technique and take maximum advantage of CMOS sensor high-speed characteristics for application such as seamless imaging that can cap-

ture still images at the same time as capturing moving images to hard disk video recorders and other devices. This technology also has the possibility of implementing new ultrahigh-speed cameras that can capture video at the ultrahigh speed of several hundred frame/s.

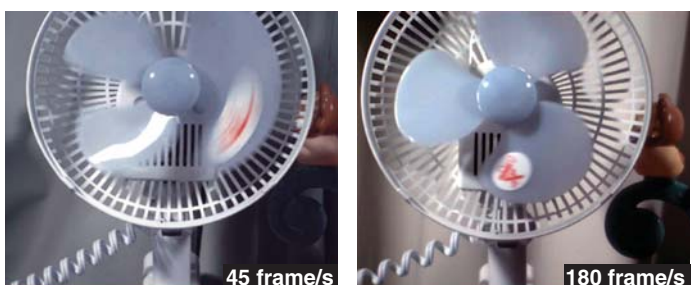
Sony is now developing products that aim at creating a new imaging world by combining the high sensitivity and high picture quality technologies created during Sony's CCD development efforts with the high-speed imaging technology that CMOS sensors can achieve. Keep your eye on Sony's ultrahigh-speed high picture quality CMOS sensors.



■ Figure 6 Chip Layout (Prototype)



■ Photograph 1 180 frame/s Sample Image



■ Photograph 2 Comparison of 45 frame/s with 180 frame/s Images